LISTING OF THE CLAIMS

Please add new claims 11-14 as indicated in the following listing of claims, which replaces all prior versions.

1. (Previously presented) A power semiconductor device, comprising:

first and second main terminals, at least one of which is for coupling a load;

a control terminal; and

a semiconductor body having opposed first and second major surfaces and a plurality of cells arranged as a lattice across the first major surface of the semiconductor body, the cells being divided into main cells and sense cells, each of the cells having a gate or base connected to the control terminal

wherein each of the main cells is connected in parallel between the first and second main terminals to couple the first and second main terminals under the control of the control terminal;

the power semiconductor device further comprises first and second sense terminals;

the sense cells are divided into a plurality of groups of sense cells each arranged across the lattice in a pattern, each group of sense cells being connected in parallel between a respective sense terminal and the second main terminal; and

a first group of sense cells is arranged across the lattice in a pattern having a different ratio of edge to inner cells to a second group of sense cells, inner sense cells being cells surrounded by other sense cells of the group and edge sense cells being arranged on the edge of the group of sense cells.

2. (Previously presented) A semiconductor device according to claim 1 wherein the number of edge sense cells in the first and second groups of sense cells is substantially identical.

3. (Previously presented) A semiconductor device according to any preceding claim wherein the cells are MOS cells including a gate-connected to the control terminal, and a source and drain, the source and drain of main cells being connected to the first and

second main terminals and the source and drain of sense cells of a group being connected between the second main terminal and the respective sense terminal.

4. (Previously presented) A semiconductor device according to claim 3 wherein the cells are trench MOSFET cells.

5. (Previously presented) A semiconductor device according to claim 1 further comprising a Kelvin terminal connected to the source of the main cells.

6. (Previously presented) A semiconductor arrangement comprising:

a semiconductor device according to claim1;

a drive circuit having an input and an output, the output being connected to the control terminal for driving the control terminal; and

a compensation circuit having first and second sense inputs connected directly or indirectly to the first and second sense terminals, respectively, and an output connected to the drive circuit for controlling the drive circuit, wherein the compensation circuit outputs to the drive circuit input a signal based on the current in inner sense cells, obtained from the currents on the first and second sense inputs.

7. (Previously presented) A semiconductor arrangement according to claim 6 wherein:

the compensation circuit includes a reference sub-circuit with an input connected to the first sense terminal connected to the first group of sense cells, and an output supplying a reference voltage, wherein the current from the first sense terminal is applied across a resistance to increase the reference voltage linearly with the current from the first group of sense cells;

the compensation circuit further includes a sense sub-circuit which has an input connected to the second sense terminal connected to the second group of sense cells wherein the current from the second group of sense cells is applied across a like resistance to that in the reference sub-circuit to generate a voltage; and

the sense sub-circuit has a compensation input connected to the output of the reference sub-circuit,

the sense sub-circuit being operable to compare the voltage input on the compensation input with that generated across the like resistor to generate an output supplying a compensated sense current signal to the drive circuit input for controlling the drive circuit to limit the current output by the power semiconductor device.

8. (Previously presented) A semiconductor arrangement according to claim 7 wherein:

the power semiconductor device has MOS cells of predetermined first conductivity type having gate, source and drain, the gates of the cells being connected in parallel to the control terminal, the drains of the main and sense cells being connected in common to the first main terminal and the sources of the main and sense cells being connected to the second main terminal and sense terminals respectively;

wherein the second main terminal is connected to a source voltage rail (V_{ss});

the drive circuit includes a FET of the first conductivity type having its source connected to the source voltage rail, its drain connected to the control terminal of the power semiconductor device and to a gate drive circuit;

the reference sub-circuit includes a FET of the first conductivity type having its source connected to the source voltage rail through the resistance, its drain connected through a resistance to a logic supply, its gate connected to its drain and to the output of the reference sub-circuit, and wherein the input of the reference sub-circuit is connected to the source of the reference sub-circuit FET for supplying the current output on the first sense terminal to the reference sub-circuit; and

the sense sub-circuit includes a FET of the first conductivity type having its source connected to the source voltage rail through the resistance, its drain connected through a resistance to a logic supply, its gate connected to the output of the reference sub-circuit, and wherein the input of the sense sub-circuit is connected to the second sense terminal for comparing the current output on the second sense terminal with a value set by the reference sub-circuit and outputting a signal to the drive circuit.

9. (Previously presented) A semiconductor arrangement according to any of claims 6 to 8 housed in a single package.

10. (Previously presented) A semiconductor arrangement according to any of claims 6 to 8 wherein the first main terminal is connected to a load.

11. (New) A semiconductor device according to claim 1 wherein the first group of sense cells includes at least as many edge cells as inner cells, and wherein the second group of sense cells includes more inner cells than edge cells

12. (New) A semiconductor device according to claim 11 wherein at least 80% of the sense cells of the first group of sense cells are edge cells.

13. (New) A semiconductor device according to claim 11 wherein the number of edge sense cells in the first and second groups of sense cells is substantially identical.

14. (New) A semiconductor device according to claim 13 further including a compensation circuit that uses a current output from the first group of sense cells to compensate a current output from the second group of sense cells to thereby provide a signal reflective of the current in inner sense cells.